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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/577,734	05/23/2000	Kouji Takagi	13624	3883

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EXAMINER
DUONG, THOI V

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 08/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/577,734	TAKAGI, KOUJI	
	Examiner	Art Unit	
	Thoi V Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,4,6,7,10-13 and 15-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,4,6,7,10-13 and 15-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to the Amendment, Paper No. 16, filed June 02, 2003.

Accordingly, claims 3, 4, 6, 7 and 10-13 were amended, claims 2, 5 and 9 were cancelled, and new claims 15-17 were added. Currently, claims 3, 4, 6, 7, 10-13 and 15-17 are pending in this application.

2. Applicant's arguments with respect to claims 3, 4, 6, 7 and 10-13 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 6 recites the limitation "said back light portion" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 7 recites the limitation "said back light portion" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 17 recites the limitation "said nitride film" in line 24 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikawa (JP 05-232509) in view of Dojo et al. (USPN 6,528,357 B2).

A shown in Figs. 2 and 3, Nishikawa discloses a liquid crystal display device as having a liquid crystal display panel, said liquid crystal display panel comprising:

a plurality of pixels which are disposed on a TFT substrate 11 in a matrix having rows and columns and each of which has at least a thin film transistor (TFT) 1 and a pixel electrode 20, each said pixel having an opening defining an aperture ratio;

a plurality of gate signal lines GL which extend from a gate signal input portion disposed along a side of said liquid crystal display panel and each of which is coupled with said TFT's in a row of said matrix;

auxiliary capacitor portions 13, CSCA, CSCB, CSCC, each additionally coupled with a pixel electrode of one of said pixels, the width of said gate signal line becomes narrower and thereby capacitance of said auxiliary capacitor portions becomes smaller as the distance from said gate signal input portion becomes larger (see Abstract);

an opposing substrate 23 which opposes to said TFT substrate while keeping a small gap therebetween, said small gap being filled with liquid crystal 27; and

the aperture ratio increasing as the capacitance of said auxiliary capacitor portions becomes smaller (Fig. 2);

capacitance of each of said auxiliary capacitor portions being determined by an area of an opposing portion between a pixel electrode of a pixel and a gate signal line coupled with an adjacent pixel via an interlayer insulating film 14 between said pixel electrode and said gate signal line (Fig. 3),

wherein an area of an aperture portion of said pixel becomes larger since the auxiliary capacitor portions become smaller, CSCA>CSCB>CSCC, as the distance from said gate signal input portion becomes larger (Fig. 2).

Nishikawa discloses a liquid crystal display device that is basically the same as that recited in claims 3 and 4 except for a nitride film disposed between said pixel electrode and said gate signal line in addition to the insulating film. As shown in Fig. 2, Dojo et al. discloses a liquid crystal display device comprising an auxiliary capacitor portion whose capacitance is determined by an area of an opposing portion between a pixel electrode 131 of a pixel and a gate signal line 111 coupled with an adjacent pixel via an interlayer insulating film 115/117 and an interlayer dielectric film 127 made of silicon nitride between said pixel electrode and said gate signal line (col. 4, lines 11-41). Dojo et al. teaches that it is possible to sucessfully suppress occurrence of electrical interlayer shorting due to this inherent structure (col. 5, lines 8-13). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD device of Nishikawa with the teaching of Dojo et al. by forming a nitride film between said pixel electrode and said gate signal line in addition to the insulating film so as to suppress occurrence of electrical interlayer shorting which affects the display quality.

9. Claims 6, 7 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikawa (JP 05-232509) in view of Dojo et al. (USPN 6,528,357 B2) as applied to claims 3 and 4 above and further in view of Taniguchi et al. (USPN 6,334,689 B1).

The LCD device of Nishikawa as modified in view of Dojo et al. above includes all that is recited in claims 6, 7 and 10-13 except for a backlight portion. As shown in Figs. 2 and 3 Prior Art, Taniguchi discloses a backlight portion employed in a conventional liquid crystal display device comprising one elongated light source 1 and a light guide plate 2 which is provided with an optical scattering layer 3 from which light is scattered. As to the optical scattering layer 3, which is shown more detail in Fig. 3, it consists of a plurality of ink dots 8, formed of optical scattering materials, arranged on the surface of light guide 2 (col. 1, lines 64-67). As the distance increase from the light source 1, the optical intensity from the light source 1 is reduced; therefore, as the distance increases from the light source 1, as shown in Fig. 3, the area of the ink dots 8 is increases (col. 2 lines 1-4). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD's device of Nishikawa as taught by Taniguchi by employing a backlight portion for illuminating said liquid crystal display panel from the backside thereof so that luminance of backlight by said backlight portion becomes lower as the distance from said gate signal input portion becomes larger so as to obtain a high image luminance and a high image display quality.

10. Claims 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikawa (JP 05-232509) in view of Dojo et al. (USPN 6,528,357 B2) as applied to claims 3 and 4 above and further in view of Applicant's Prior Art (Fig. 12 and Equation 6).

As shown in Figs. 2 and 3, Nishikawa further discloses that said pixels of the liquid crystal display device each correspond to an equivalent circuit comprising:

a drain coupled to a drain signal line DL, said drain signal line having a gate coupled to said gate signal line; and

a source corresponding to said pixel electrode coupled to an opposing electrode 25 disposed on a substrate 23, said pixel electrode having a gate coupled to said gate signal line.

The LCD device of Nishikawa as modified in view of Dojo et al. above includes all that is recited in claims 15 and 17 except for the formula for calculation of storage capacitance at a distance from the gate line input portion. As shown in Fig. 12, Applicant's Prior Art discloses an equation 6 for obtaining the storage capacitance at the portion C which is further away from a gate input terminal 2 (see Specification, Background of the Invention):

Csc' = [{(Cgs)(DeltaVg) - S Ids dt} {Clc + Csc + Cgs }] / {(Cgs)(DeltaVg)} - (Clc - Cgs), wherein

said pixel electrode and said gate have a corresponding gate source capacitance, Cgs,

said pixel electrode and said opposing electrode have a corresponding liquid crystal capacitance, Clc,

said pixel electrode overlapping said gate signal line form a corresponding storage capacitance, Csc,

differences in amplitude of the gate signals defining a gate pulse amplitude, DeltaVg,

a total TFT leakage current flowing from said pixel electrode to said drain signal line until said TFT current is completely dissipated being defined as S Ids dt;

and variation of storage capacitance, Csc, with distance from said gate signal line being defined as Csc'.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to apply Equation 6 of the Applicant's Prior Art to determine the relationship between storage capacitance values Csc and Csc'.

11. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikawa (JP 05-232509) in view of Dojo et al. (USPN 6,528,357 B2) and Taniguchi et al. (USPN 6,334,689 B1) as applied to claims 6, 7 and 10-13 above and further in view of Applicant's Prior Art (Fig. 12 and Equation 6).

As shown in Figs. 2 and 3, Nishikawa further discloses that said pixels of the liquid crystal display device each correspond to an equivalent circuit comprising:

a drain coupled to a drain signal line DL, said drain signal line having a gate coupled to said gate signal line; and

a source corresponding to said pixel electrode coupled to an opposing electrode 25 disposed on a substrate 23, said pixel electrode having a gate coupled to said gate signal line.

The LCD device of Nishikawa as modified in view of Dojo et al. and Taniguchi et al. above includes all that is recited in claim 16 except for the formula for calculation of storage capacitance at a distance from the gate line input portion. As shown in Fig. 12, Applicant's Prior Art discloses an equation 6 for obtaining the storage capacitance at the

portion C which is further away from a gate input terminal 2 (see Specification, Background of the Invention):

Csc' = [{(Cgs)(DeltaVg) - S Ids dt} {Clc + Csc + Cgs }] / {(Cgs)(DeltaVg)} - (Clc - Cgs), wherein

said pixel electrode and said gate have a corresponding gate source capacitance, Cgs,

said pixel electrode and said opposing electrode have a corresponding liquid crystal capacitance, Clc,

said pixel electrode overlapping said gate signal line form a corresponding storage capacitance, Csc,

differences in amplitude of the gate signals defining a gate pulse amplitude, DeltaVg,

a total TFT leakage current flowing from said pixel electrode to said drain signal line until said TFT current is completely dissipated being defined as S Ids dt;

and variation of storage capacitance, Csc, with distance from said gate signal line being defined as Csc'.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to apply Equation 6 of the Applicant's Prior Art to determine the relationship between storage capacitance values Csc and Csc'.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (703) 308-

3171. The examiner can normally be reached on Monday-Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (703) 305-3492.

Thoi Duong

07/30/2003

T. Chowdhury
Primary Examiner